Design and Implementation of Visual System Based on FPGA

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Abstract: In this paper, a scheme of vision system based on FPGA is proposed. The vision system takes FPGA as the control core, this paper first converts the RGB image into YCBCR format, extracts the Y component to complete the grayscale processing of the image, and then realizes the realization of the Sobel operator on the FPGA. This design makes full use of the advantages of FPGA in parallel processing, and realizes the edge detection of the target object by Sobel algorithm.

1. Introduction

Vision system refers to the target is converted into image signal through machine vision, transmitted to the special image processing system, and then according to the pixel distribution and brightness, color and other information, it is transformed into an easy to process digital signal, the image system of these signals to carry out a variety of operations to extract the characteristics of the target, Then according to the results of the discrimination to control the site of the device action [1].

Vision system is generally composed of three main parts: Image acquisition, processing and analysis and output, commonly used vision system in the general computer platform for visual information processing, but due to the limited computing power of the CPU, some computational complexity of the visual algorithm, its processing speed is often difficult to meet the real-time needs of the system [2]. Because of the characteristics of parallel computing, the vision system based on FPGA can not only meet the performance requirements of high-speed processing of visual information, but also further reduce power consumption, which is a good way to avoid the defects of conventional vision system, and is an excellent solution to realize robot vision system. With the further improvement of FPGA integration, FPGA will be an important development direction of robot vision system. [3].

2. Design Of Vision System Based On Fpga

In this paper, Altera's Cyclone series of ep4ce10e22c8n FPGA as the core, the use of Quartus II software. Through the OV7725 camera acquisition image, using FPGA to complete the image data capture, internal video image algorithm processing optimization, asynchronous image data cache transmission and VGA driver complete brush screen display, and finally through the VGA interface on the display to get real-time capture of the image screen, and add algorithm optimization, Enables the detection of the edges of an object [4]. The system block diagram is shown in Figure 1:

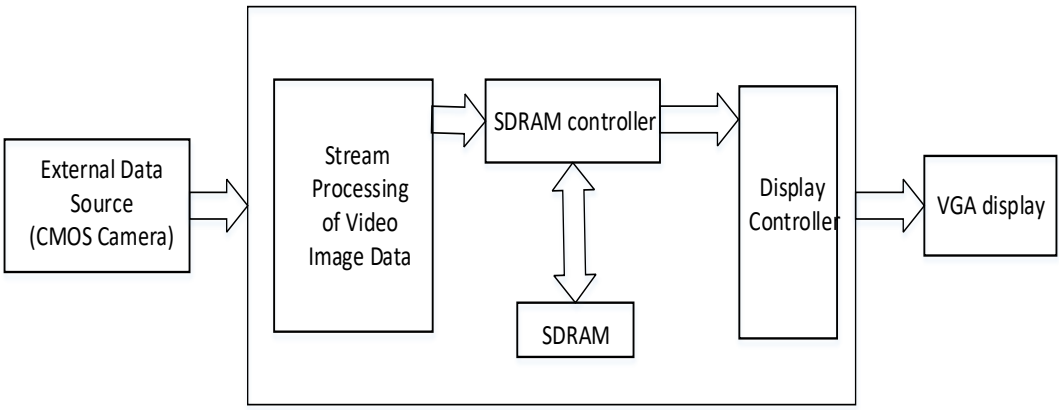


Figure 1. System control block diagram

The process of obtaining data flow throughout the system is to complete the acquisition of external image data through the CMOS data capture module after the CMOS camera completes initialization, and then the FPGA processes the acquired data flow initially, and completes the signal synchronization and writes it to the SDRAM module. The SDRAM storage module is used as the high speed data flow channel, and finally the externally collected image data is refreshed and output on the VGA display in real time through multi-frame refresh. In this paper, OV7725 CMOS sensor is selected as the video image source. The internal use of 640*480 photosensitive array, can achieve the fastest 60fps VGA resolution per second video, and resolution, output data format, image characteristics, etc. can be freely configured by the user. The physical figure of OV7725 is shown in Figure 2.

Figure 2. OV7725

The SCCB of OV7725 is similar to I2C communication bus, the two signal interfaces are the clock signal SCL and the data signal SDA, through which the two signal interfaces can communicate with the sensor and complete the configuration of the internal register to achieve the expected video stream output.

3. HDL Realization of Visual System Modules

3.1 Camera module

3.1.1 Initialization of OV7725 Communication Interface

The SCCB provided by OV7725 is serial bus, Communication can be achieved with only two wires, of which Sdat is a serial data cable and SCLK is a serial clock line. Before implementing communication, it is necessary to complete the initialization of SCCB, generate clock control signal, the process is shown in Figure 3.

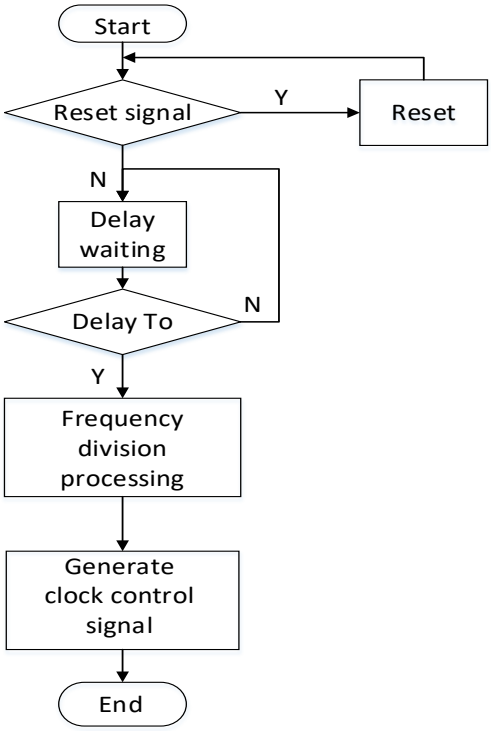


Figure 3. SCCB Initialization flow chart

3.1.2 Initialization of OV7725 Communication Interface

OV7725 has a total of 172 registers to configure the operating mode of the CMOS sensor, and the register must be initialized before the sensor is working properly, otherwise the image of the expected Fig. quality cannot be obtained. On the basis of implementing the above SCCB bus protocol, some important registers in 172 registers need to be configured. Configure the parameters of the OV7725 register, need to complete the reading and writing operation of the register according to a certain process, the two modes operate as follows:

(1) Write operation

SCCB bus in the write register, first write the device address (write ID address is 0x42, read ID address is 0x43), then write the register address, and finally write the value of the register, so that complete the configuration of a register, that is, ID_Address + SUB_Address + W_Data process.

(2) Read operation

Write the device address ID_Address (0x42) First, then write the register address SUB_Address that needs to be read, read the ID address ID_Address (0x43), and finally read the value R_Data of the specified register within the CMOS sensor.

3.1.3 OV7725 Acquisition interface

In this paper, 16 bits of True color external image data are collected by CMOS sensor, that is, the acquisition of RGB565 data is completed. RGB565 that is {R [4:0], G [5:0], B [4:0}, When VSYNC and HREF are effective, Each PCLK clock first sends RGB565's high 8-bit {R [4:0], G [5:3]}, Then send the RGB565 low 8-bit {G [2:0], B [4:0]}. To read the full 16-bit RGB565 data, you need to stitch the adjacent two Data when the HREF line synchronization signal is valid [5]. RTL The view is shown in Figure 4:

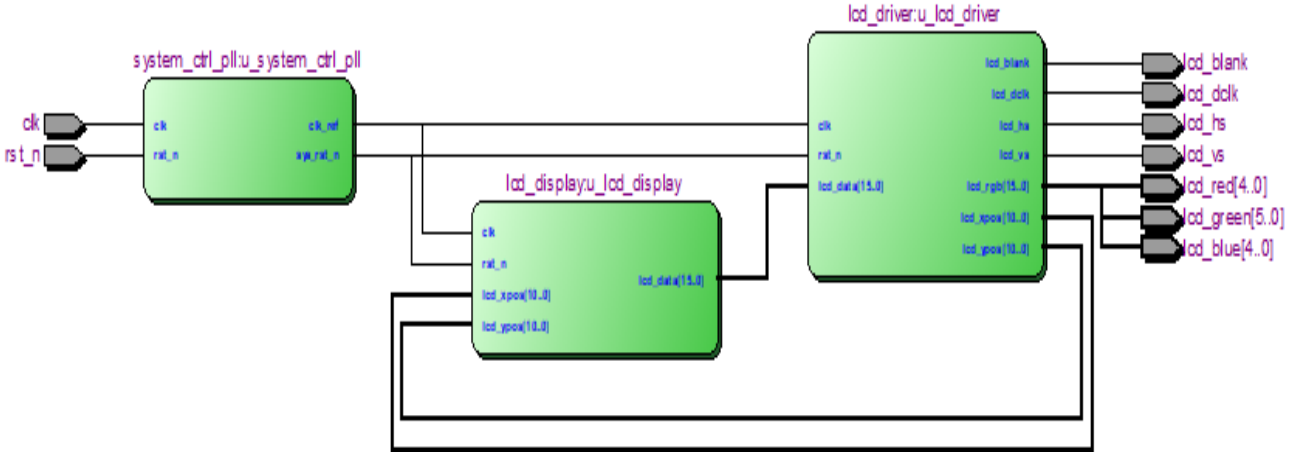


Figure 4. RTL view after VGA instantiation

3.2 SDRAM controller

Typically, each storage unit can hold data with a bit width of 8/16/32, which is a combination of blocks called logical Bank, while most SDRAM chips are designed internally with 4 bank. Therefore, the addressing process is often: chip selection, specified chip → Specify the Bank address → Specify the line address → specify the column address → determine the addressing unit [6]. Once the storage unit is found, the final data transfer is performed.

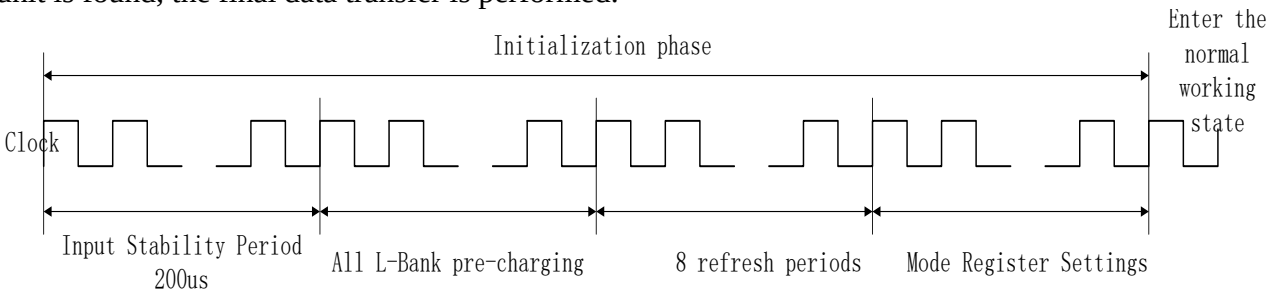


Figure 5. Chip initialization sequence diagram

After power-on, the chip is first initialized and the process is shown in Figure 5. Maintain a 200US input stabilization period at boot time, then complete all l-bank pre-charging in about 20 clock cycles, complete 8 refresh periods, and finally load the configuration of the mode register. When initialization is complete, it is addressed against the column to complete the reading and writing of the data.

4. Debugging of Visual System

CMOS camera as an external data source of images, after FPGA data processing, signal synchronization, data caching, the corresponding 16-bit wide RGB565 data, through the VGA display, the realization of real-time system image acquisition, physical platform as shown in Figure 6.

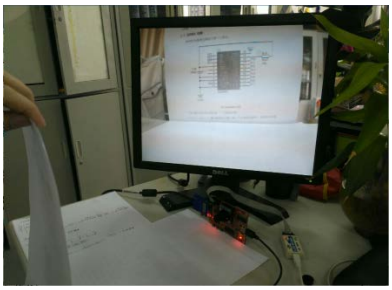


Figure 6. Real-time image acquisition by robot vision system

4.1 VGA Display Module Testing

System debugging according to the module to test whether its function is normal, first of all, the VGA display module. Write test code internally to output color stripes to detect if the VGA interface is working correctly, as shown in Figure 7 and Figure 8.

Figure 7. Color Cross Stripes

Figure 8. Color Vertical Stripe

4.2 Implementation of Sobel operator on FPGA

4.2.1 Grayscale processing

This paper uses the output RGB data, the RGB model display fits the color that the human eye can recognize, but it fuses the hue, brightness and saturation together, it is difficult to separate, is not conducive to the later digital processing. In order to facilitate edge detection of objects and realize feature extraction, it is necessary to convert RGB into grayscale image and reduce the computation of image processing. The scheme used in this paper is to convert RGB into YCbCr, and then extract Y component to realize the transformation of grayscale image [7].

For the YCbCr color space, the Y component is the brightness signal of the image, CB and CR are the blue and red chromatic aberration signals in the image data, in the grayscale image conversion, only the Y channel is required. The conversion of RGB and YCbCr is as follows:

$Y = 0.299R + 0.587G + 0.114B;$

$Cb = -0.1687R - 0.3313G + 0.5B + 128;$

$Cr = 0.5R - 0.4187G - 0.0813B + 128.$

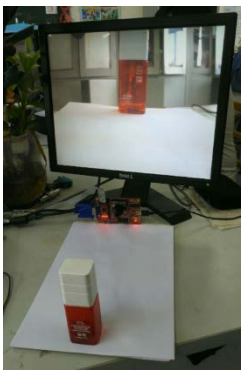


Figure 9. Color before addition

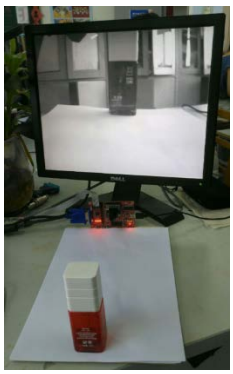


Figure 10. Gray Level Display by Adding Algorithms

4.2.2 Edge Detection Algorithms

Edge is a set of points in which pixel grayscale changes dramatically in digital images, and edge detection is to extract the edges of the target in the image by algorithm, because there is a brightness contrast between the target and the background, and an area can be determined according to the closed edge, which is the contour of the detection target.

The common methods of edge detection are Sobel operator, Prewitt operator, Roberts cross operator, etc., this paper uses Sobel edge detection algorithm, which is a first-order discrete difference operator, which is used to calculate the grayscale gradient in the image. The operator contains two sets of 3*3 matrices, both transverse and longitudinal, which are planar convolution with the image, and the luminance difference approximations of the transverse and longitudinal

values can be obtained respectively. If a represents the original image, Gx and Gy represent the grayscale values of the transverse and longitudinal edges, respectively, with the following formulas (1) and (2):

$$G_x = \begin{bmatrix} -1 & 0 & +1 \\ -2 & 0 & +2 \\ -1 & 0 & +1 \end{bmatrix} * A \tag{1}$$

$$G_y = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 \\ -1 & -2 & +1 \end{bmatrix} * A \tag{2}$$

For Gx and Gy, the grayscale value of the corresponding pixel point can be obtained, as shown in formula (3).

$$G = \sqrt{G_x^{\,2} + G_y^{\,2}} \tag{3}$$

Finally, the threshold value is set, and when the grayscale value G is greater than the set value, the point (x, y) is considered to be the edge point and the effective value is output. The Sobel operator is partially instantiated as shown in figure 11 below

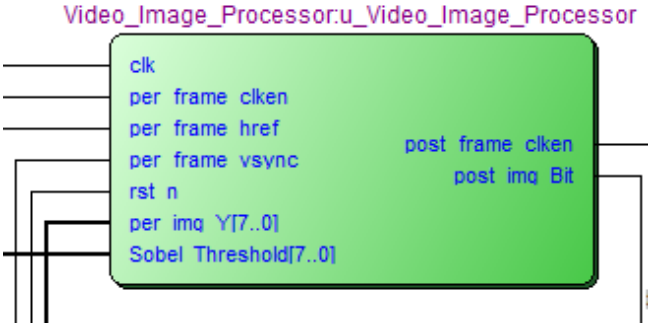


Figure 11. RLT Diagram of Sobel Operator Image Processing Module

Among them, CLK is the signal input interface of the global clock; Rst_n is the global reset signal; Per_frame_clken, Per_frame_href and Per_frame_vsync are the effective clock of the frame, the effective clock of the row pixel and the effective clock of the field pixel, respectively, Signal synchronization for image data processing; per_img_Y is the Y signal in the extracted YCbCr image format, that is, the grayscale image; Post_frame_clken is the output frame effective clock, post_img_Bit is the image data processed by the algorithm, Directly through the SDRAM output to the VGA, on the display display extracted to the edge.

Sobel_Threshold is a set threshold, in order to achieve the threshold dynamic adjustment, the addition of keyboard scanning function, with two keys K1, K2 to control the increase and decrease of the threshold, can be used in the system as needed to adjust the threshold size to adapt to different degrees of edge extraction, This is shown in Figure 12:

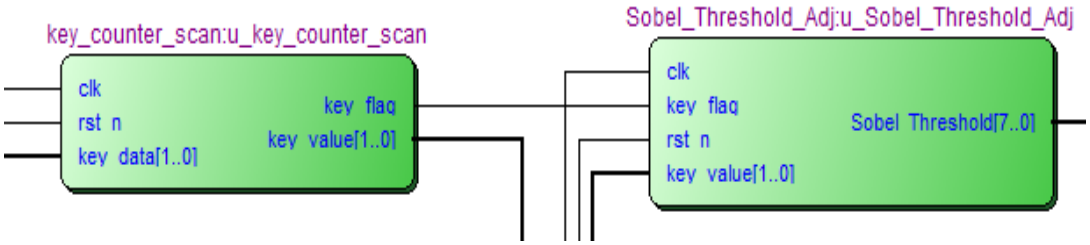


Figure 12. Threshold adjustment of Sobel operato

The RTL of the final system is shown in Figure 13:

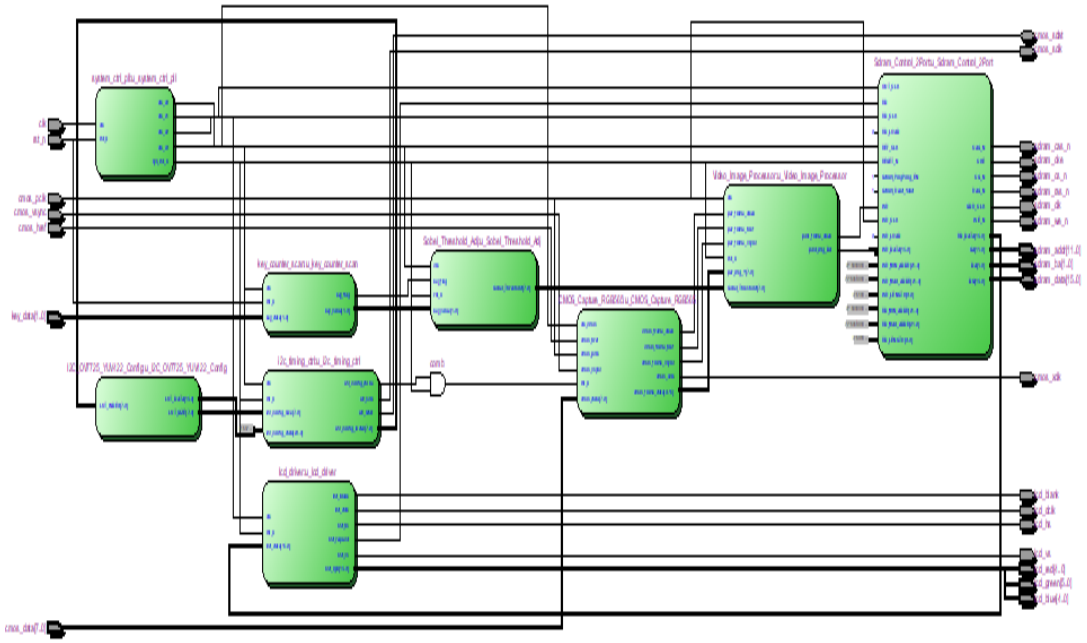
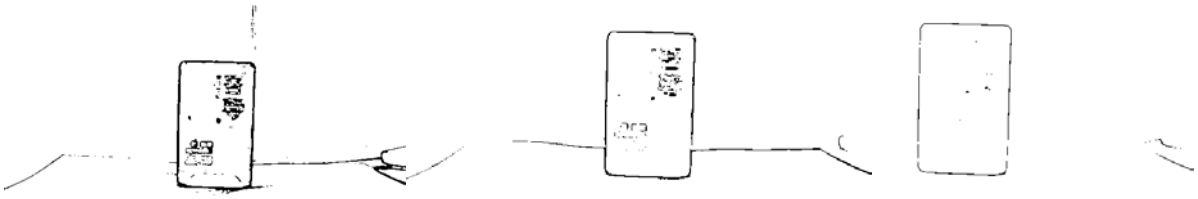


Figure 13. RLT Diagrams of Systems under Sobel Operation



(a) (b) (c)

Figure 14. Adjust the threshold of edge extraction

By adjusting the threshold extracted by the edges, when the threshold is tuned to a smaller (20), the extracted edges are shown in figure (a), showing that there are more contour details of the target at this time, and when the threshold is moderate (55), the details in figure (b) are much less than (a), preferring to extract rough contours, and when the threshold is large (90), As shown in figure (c), the text in the middle of the target has been omitted, leaving only the contours on the edge.

5. Summary

In the design process of vision system, this paper first analyzes the function, then completes the HDL realization of each module on the FPGA platform, integrates it into the system and debugging, finds the problem and solves it in the debugging, completes the basic goal of image acquisition, and finally adds the edge detection Sobel operator, The contour extraction of the detection target is completed, and the final visual design and realization are formed.

Acknowledgments

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